

Key Parameters

V_{RRM}	1600~1800	V
$I_{T(AV)}$	160	A
I_{TSM}	4.5	kA
V_{TO}	0.93	V
r_T	1.15	mΩ

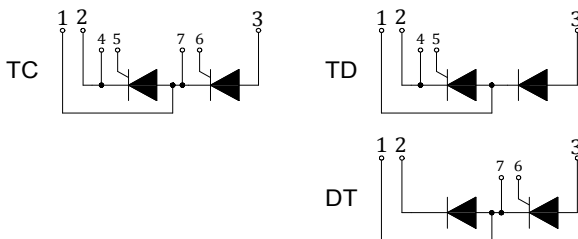
Applications

- Various rectifiers
- DC supply for PWM inverter
- Industry converter

- 3000 V_{RMS} isolating voltage with baseplate
- High power capability
- Industrial standard package

Voltage Ratings

Device Type	$V_{DRM}/V_{RRM}(V)$	Test Conditions
TMTC 160	1600 1800	$T_{vj} = 25, 130\text{ }^{\circ}\text{C}$ $I_{DRM} = I_{RRM} = 40\text{ mA}$ $V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$ $t_p = 10\text{ ms}$ $V_{DSM} = V_{DRM}$ $V_{RSM} = V_{RRM} + 100$


Thermal & Mechanical Data

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
$R_{th(j-c)}$	Thermal Resistance junction to case	sine.180°, per chip / per module DC , per chip / per module	-	-	0.2 / 0.1 0.19/ 0.095	K / W
$R_{th(C-H)}$	Thermal resistance case to heatsink	per chip / per module	-	-	0.06 / 0.03	K / W
T_{vj}	Maximum junction operating temperature range		-40	-	130	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-40	-	120	$^{\circ}\text{C}$
F	Busbar to module M6	Mounting torque $\pm 10\%$	-	6	-	N·m
	Module to heatsink M6		-	6	-	N·m
W	Weight		-	320	-	g

Current Ratings

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
$I_{T(AV)}$	Mean on-state current	Half Sine Wave, $T_c=85^{\circ}\text{C}$	-	-	160	A
$I_{T(RMS)}$	RMS on-state current	$T_c=85^{\circ}\text{C}$	-	-	251	A
I_{TSM}	Surge on-state current	$t_p=10\text{ms}$, Half Sine Wave, $T_{vj}=130^{\circ}\text{C}$, $V_R=0$	-	-	4.5	kA
I^2t	Limiting load integral	Sine Wave, $t_p=10\text{ms}$	-	-	10.1	$10^4\text{A}^2\text{s}$

Characteristics

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
V_{TM}	Peak on-state voltage	$T_{vj} = 25\text{ }^{\circ}\text{C}$, $I_{TM} = 500\text{ A}$	-	-	1.75	V
I_{DRM}	Forward leakage current	$T_{vj} = 25\text{ }^{\circ}\text{C}$, $130\text{ }^{\circ}\text{C}$, V_{DRM}/V_{RRM}	-	-	40	mA
I_{RRM}	Reverse leakage current	$a.c.$; 50 Hz ; $r.m.s.$; $t=1\text{ min}$	-	3000	-	V
V_{TO}	Threshold voltage	$T_{vj} = 130\text{ }^{\circ}\text{C}$	-	-	0.93	V
r_T	Slope resistance	$T_{vj} = 130\text{ }^{\circ}\text{C}$	-	-	1.15	m Ω
I_H	Holding current	$T_{vj} = 25\text{ }^{\circ}\text{C}$	-	-	200	mA
I_L	Latching current	$T_{vj} = 25\text{ }^{\circ}\text{C}$	-	-	1000	mA

Dynamic Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
dv/dt	Critical rate of rise of off-state voltage	$T_{vj} = 130\text{ }^{\circ}\text{C}$, $Exp.$ to $0.67 V_{DRM}$	1000	-	-	V/ μs
di/dt	Critical rate of rise of on-state current	$T_{vj} = 130\text{ }^{\circ}\text{C}$, $V_{DM} = 0.67 V_{DRM}$, $f = 50\text{ Hz}$ $I_{TM} = 1000\text{ A}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$	-	-	150	A/ μs
t_q	Turn-off time	$T_{vj} = 130\text{ }^{\circ}\text{C}$, $V_{DM} = 0.67 V_{DRM}$, $I_T = 1000\text{ A}$ $dv/dt = 20\text{ V}/\mu\text{s}$, $V_R = 200\text{ V}$, $-di/dt = 10\text{ A}/\mu\text{s}$	-	150	-	μs
Q_{rr}	Reverse Recovery Charge	$T_{vj} = 130\text{ }^{\circ}\text{C}$, $-di/dt = 10\text{ A}/\mu\text{s}$, $I_T = 1000\text{ A}$, $V_R = 200\text{ V}$	-	1000	-	μC

Gate Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
I_{GT}	Gate trigger current	$T_{vj} = 25\text{ }^{\circ}\text{C}$	-	-	300	mA
V_{GT}	Gate trigger voltage	$T_{vj} = 25\text{ }^{\circ}\text{C}$	-	-	3	V
V_{GD}	Gate non-trigger voltage	$T_{vj} = 130\text{ }^{\circ}\text{C}$, $V_D = 0.4 V_{DRM}$	0.3	-	-	V
V_{FGM}	Peak forward gate voltage		-	-	12	V
V_{RGM}	Peak reverse gate voltage		-	-	5	V
P_{GM}	Gate peak power losses		-	-	20	W
$P_{G(AV)}$	Gate average power losses		-	-	4	W

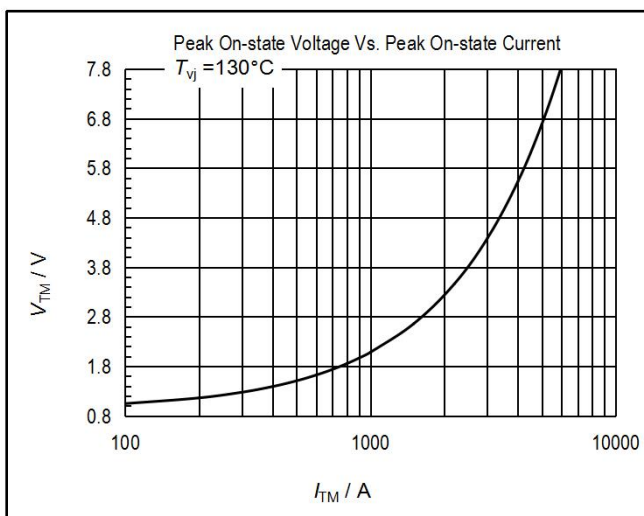


Fig1. Peak on-state Voltage Vs. Peak On-state Current

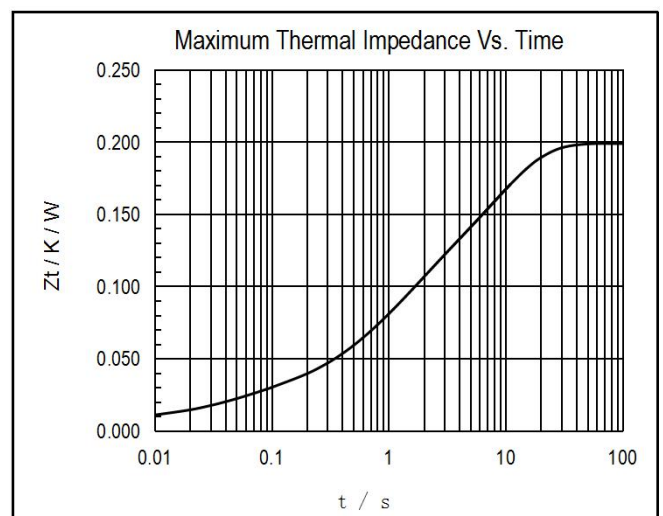


Fig2. Transient thermal Impedance Vs. Time

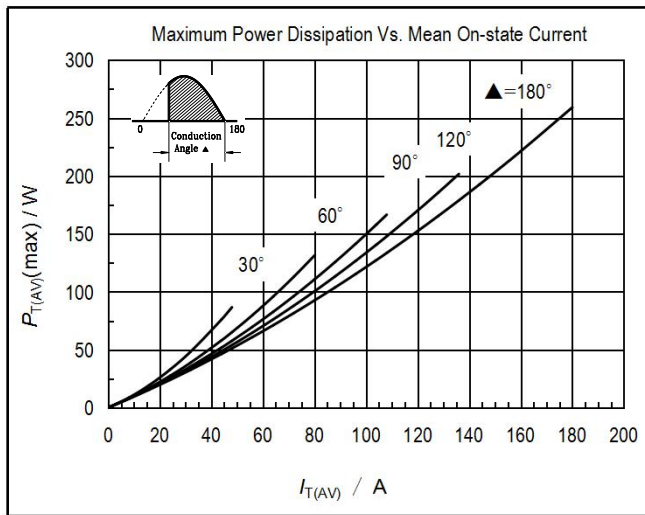


Fig3. Maximum Power Dissipation Vs. Mean On-state Current

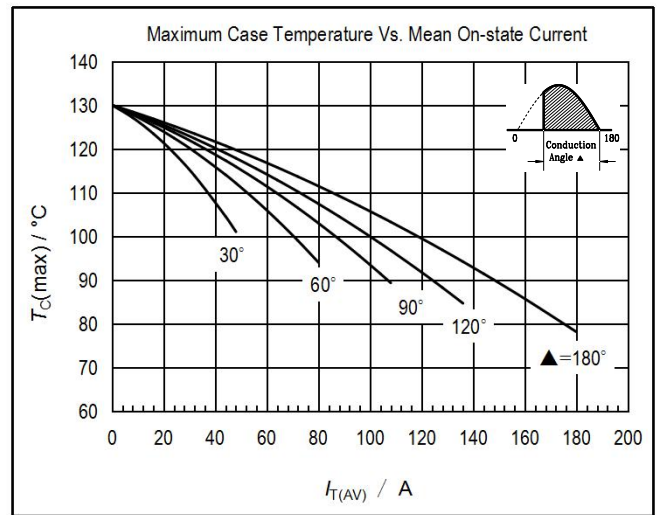


Fig4. Maximum Case Temperature Vs. Mean On-state Current

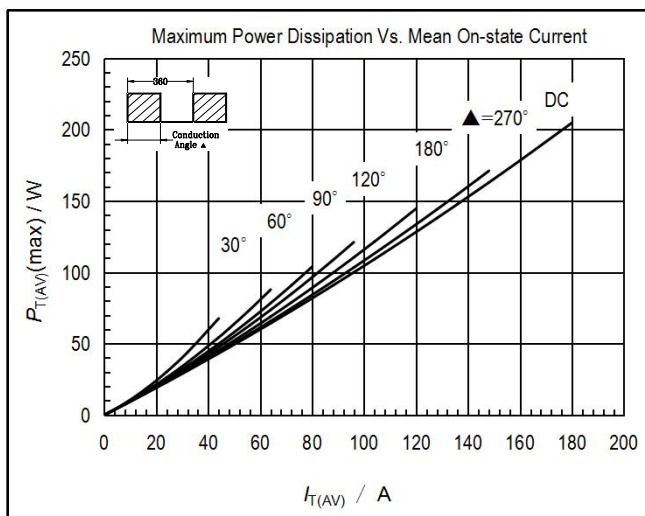


Fig5. Maximum Power Dissipation Vs. Mean On-state Current

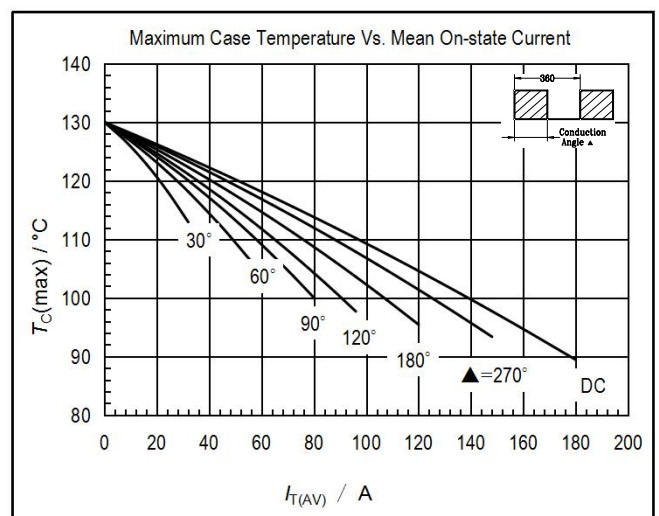


Fig6. Maximum Case Temperature Vs. Mean On-state Current

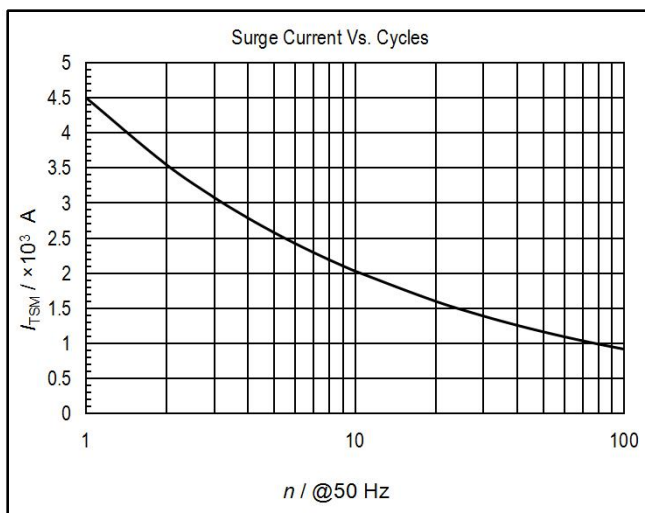


Fig7. Surge Current Vs. Cycles

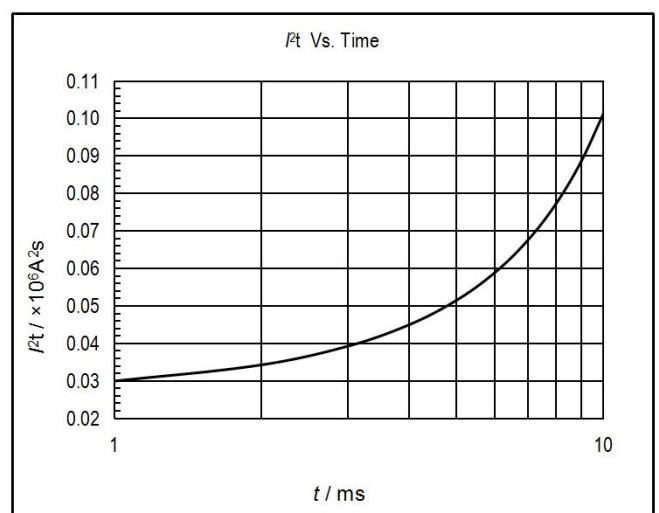


Fig8. I^2t Vs. Time

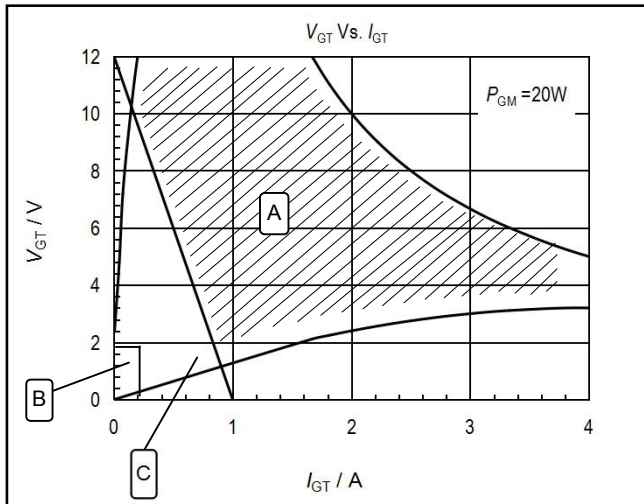


Fig9. V_{GT} Vs. I_{GT}

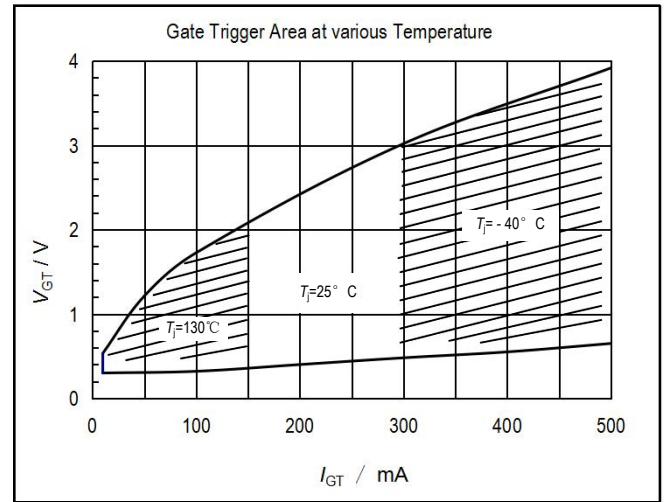


Fig10. Gate Trigger Area at various Temperature

A is Recommended Triggering Area.
B is Unreliable Triggering Area.
C is Recommended Gate Load Line.

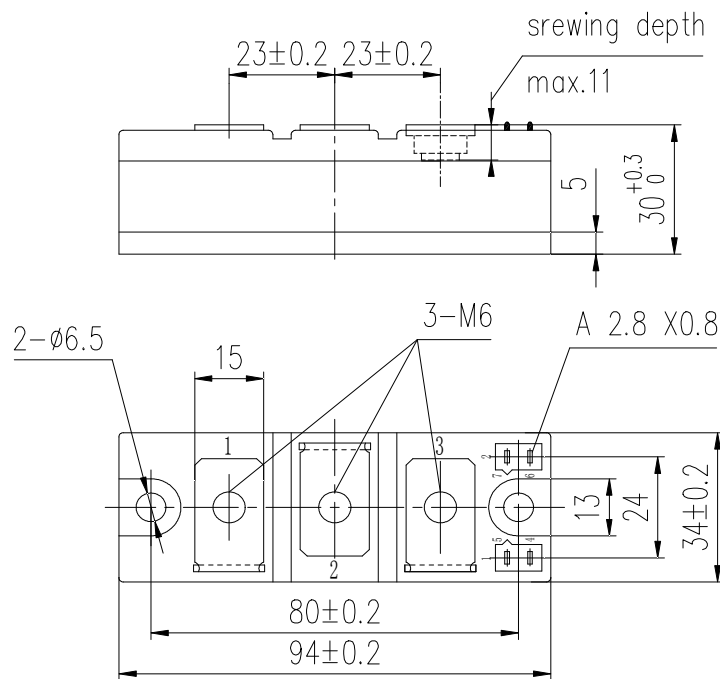


Fig9.Outline

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